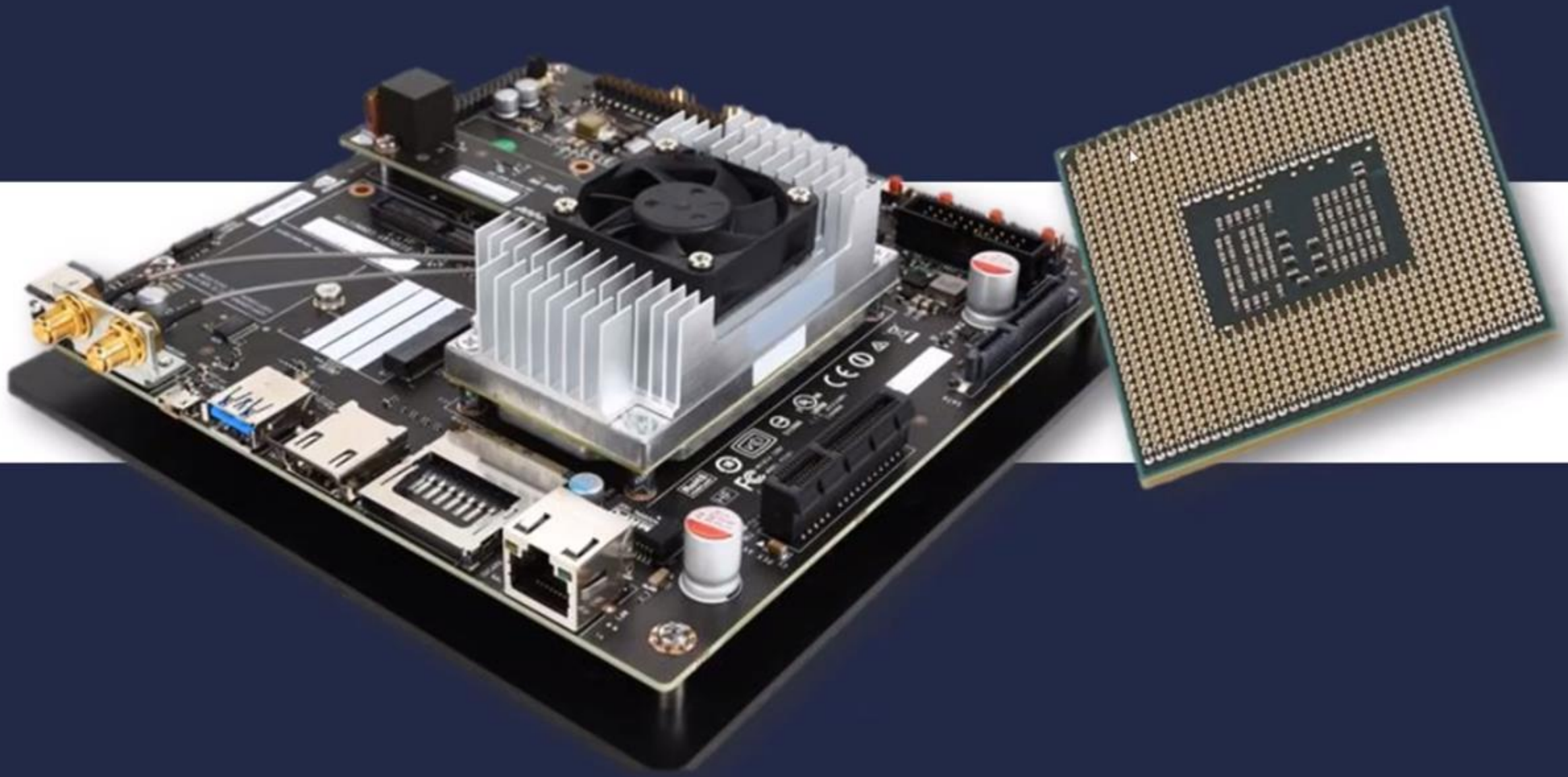
Von Neumann



CPU = Central Processing Unit

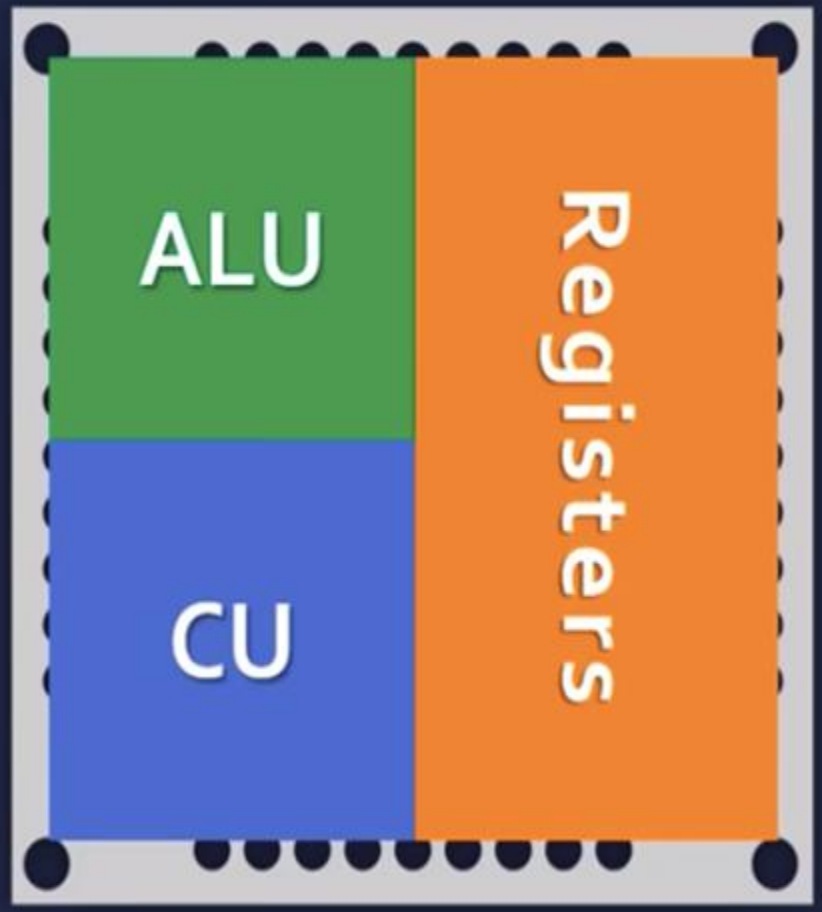
...the circuitry that controls the **manipulation of data**

Arithmetic/Logic Unit

The circuits that perform the operations on the data

Control Unit

The circuits coordinating the activities of the CPU

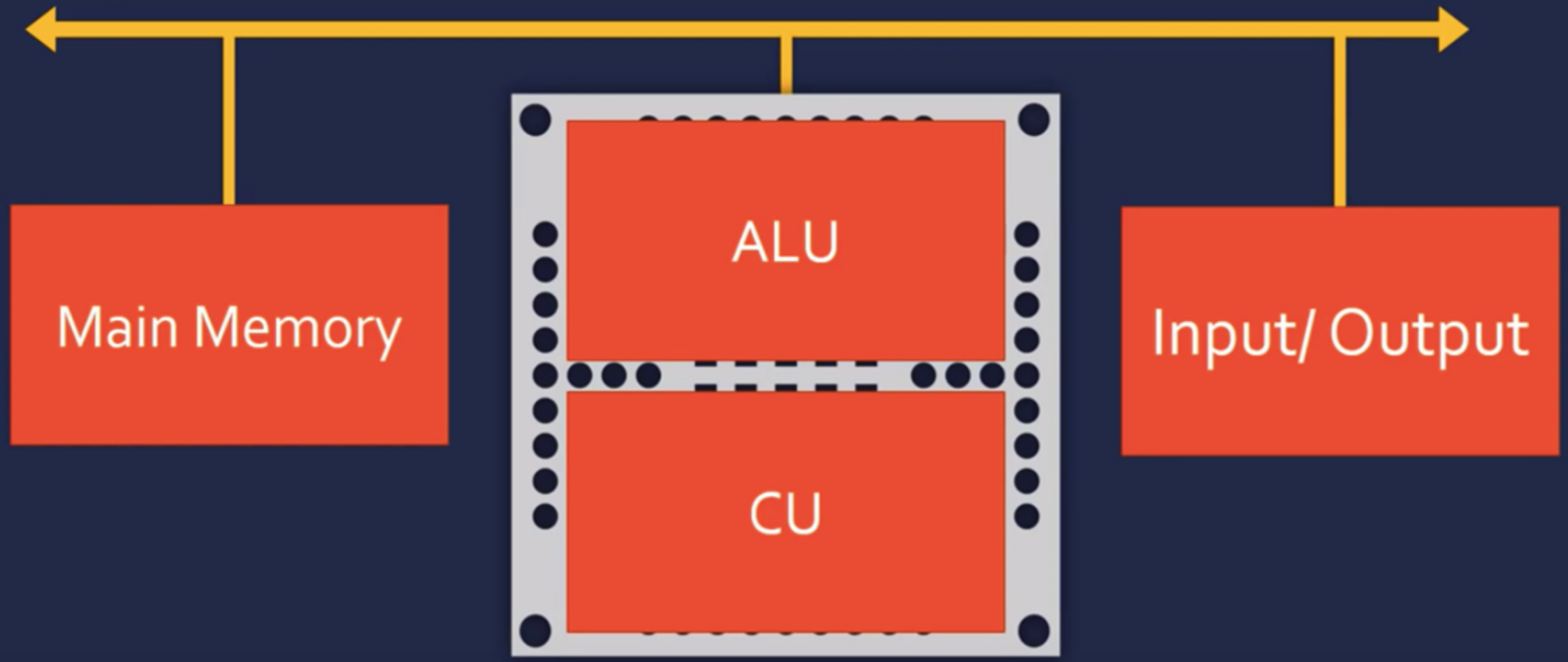


Registers

Quick, small stores of data within the CPU

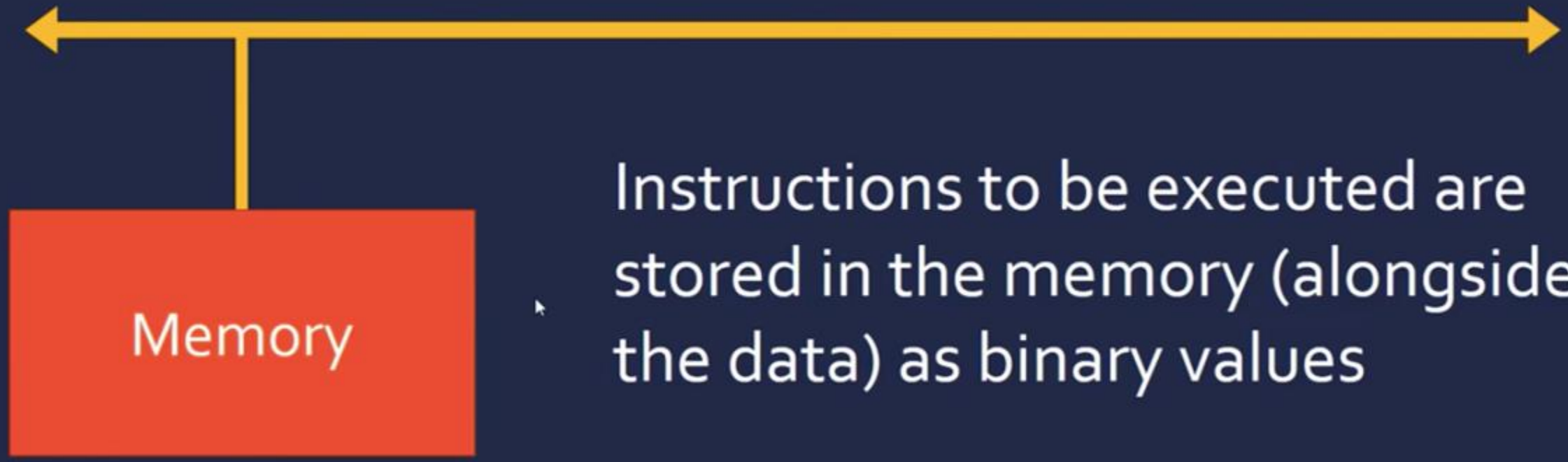
Von Neumann Architecture

- 3 major characteristics of this theoretical model…



Von Neumann Architecture

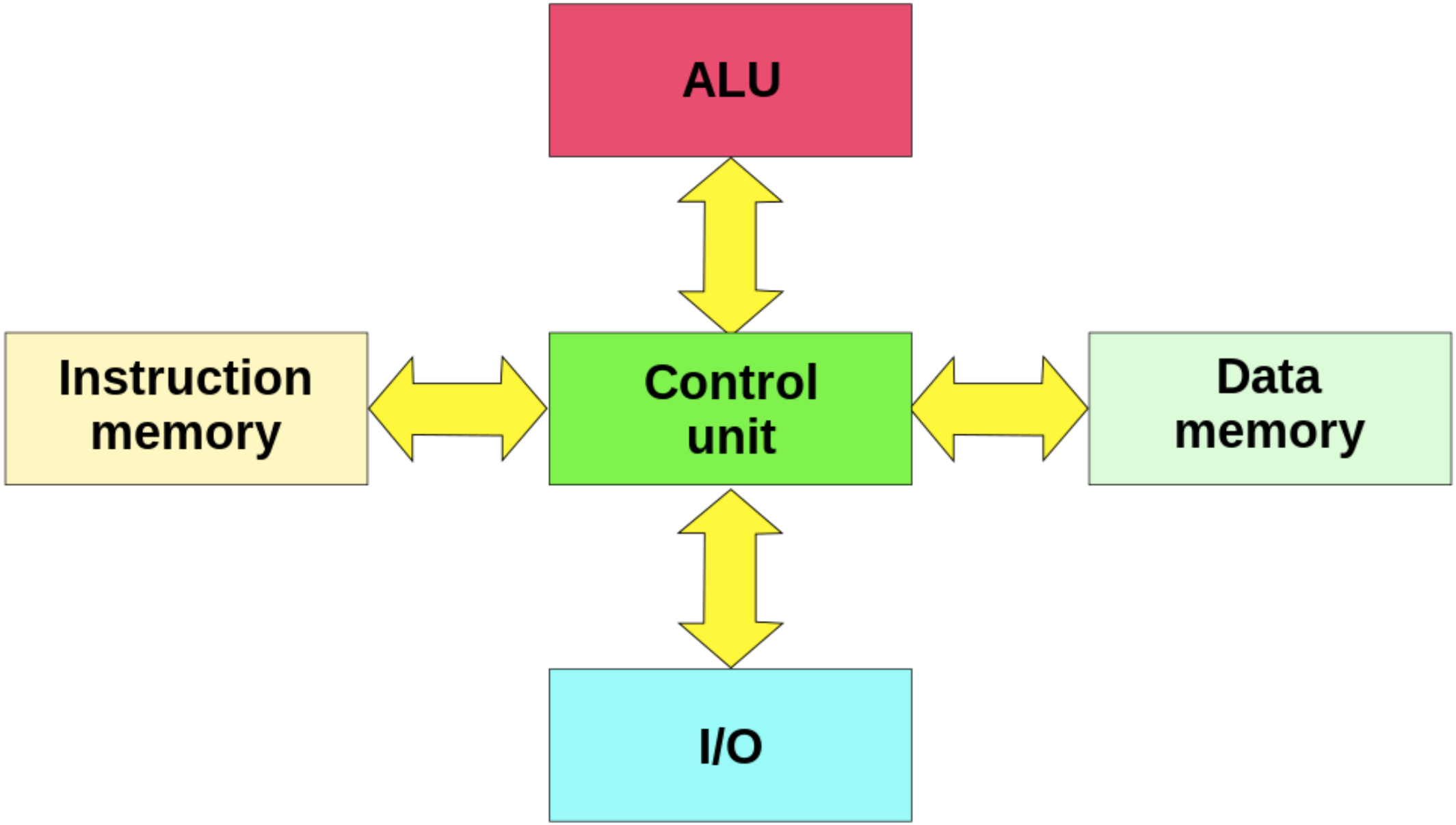
- 3 major characteristics of this theoretical model...



Instructions to be executed are stored in the memory (alongside the data) as binary values

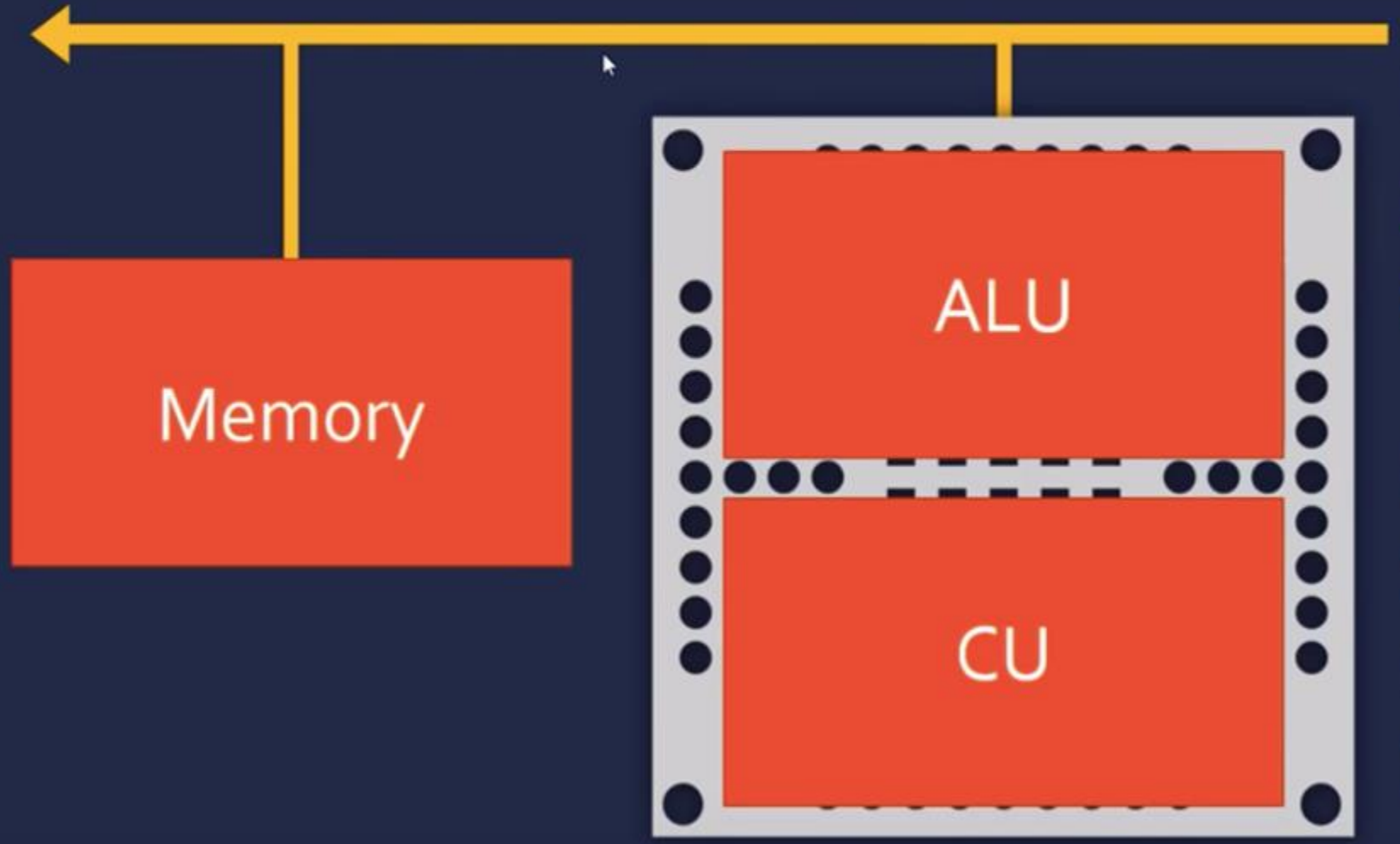
= the stored program concept

Other aspects of the Harvard model are implemented in modern CPUs though


ALU
Instruction memory
Control unit
Data memory
I/O

Von Neumann Architecture

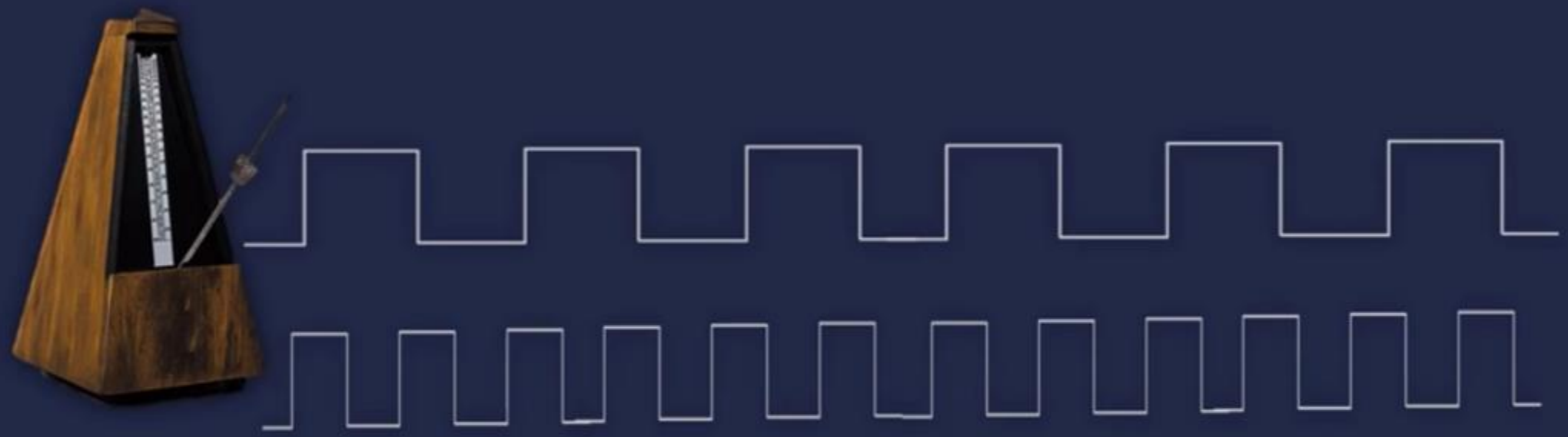
- 3 major characteristics of this theoretical model…



Instructions are **executed sequentially**:

One instruction at a time is fetched from memory and passed to the CPU

- Computers have a system **clock** which provides timing signals to synchronise circuits.



- CPUs are designed to operate at a specific frequency – and the system clock is raised to this rate by the processor, giving the **clock speed** (Hz)

- The CPU needs a certain amount of clock **ticks/cycles** per instruction

Fetch-Execute Cycle

Fetch

The next instruction is retrieved by the CPU from main memory.

Decode

`operator + operand e.g. ADD R1 R5`

The instruction is broken down to its individual components to determine what the instruction is, and what data is being used.

Execute

The CU activates the necessary circuity/ data transfers. The output of this stage is stored in a register, and data may be read/written from/to the main memory during this stage.